Machine Learning Models for Improving Productivity in ASIC Design Flow

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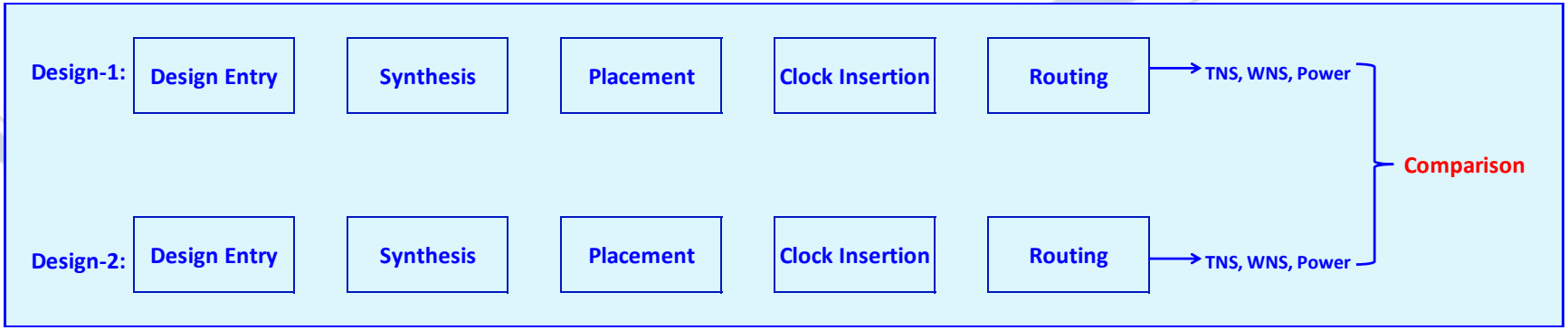
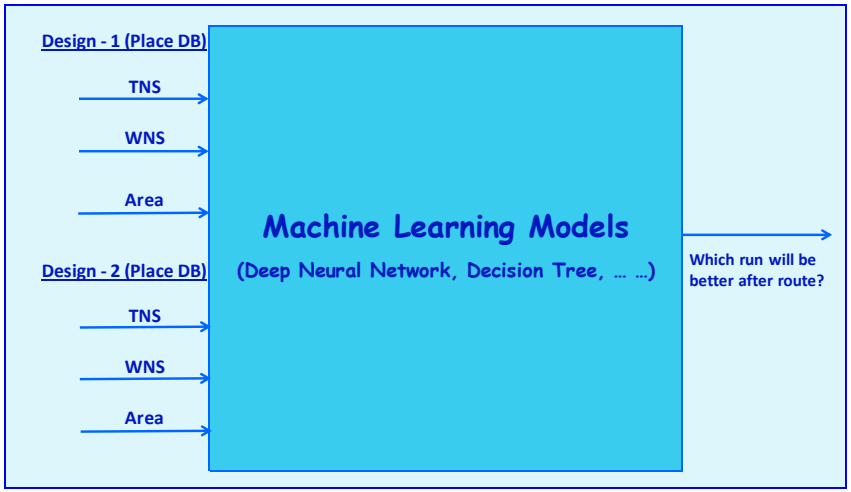
Motivation

- To achieve target Power-Performance-Area (PPA) within the goal-to-market constraint, ASIC Physical Implementation (PI) engineers run parallel experiments that target different aspects of design and/or tool settings.
- These experiments go through time-consuming and computationally expensive steps: synthesis, place, clock-insertion, route. Typical large designs may take 4-5 days to go from place to route, or even longer at early design phase.
- Rather than waiting on the final routed designs, PI engineers spend significant time to identify which of the parallel experiments will be the best one. They then pursue further improvement on those experiments. Furthermore, once the route step is finished, designers' assumptions may be proven to be incorrect.



Proposed Model

- We coin our Machine Learning (ML) based model as “CompareApp”. The model essentially targets a classification problem. We use ML-based techniques to compare two runs after place and predict which of the parallel experiments will be the best after final step (route)
- We investigate a range of models for our work:
  - Support Vector Machine (SVM)
  - Decision Tree
  - Multilayer Perceptron (MLP)
  - Deep Neural Network (DNN)



Methodology / Experimental Setup

- **Inputs:** Our Machine Learning (ML) model will take quality metrics for two placed database as inputs. Examples of such inputs are worst negative slack (WNS), total negative slack (TNS), area etc. We use a total of 84 features for two runs combined.
- **Training & Testing data:** Of the datasets collected, we *randomly* choose 90% of data for training and the remaining 10% of data for testing.
- **Output:** Our ML model will predict which run is better after the route step. We currently use only TNS for making comparison. Incorporation of other metrics into the model is a work-in-progress.
- **Tools used:**
  - We use a commercially available place-and-route tool for collecting actual data.
  - We implement our model using an ML platform, which we are developing in collaboration with Inzone.ai.

Experimental Results

- We investigate the usefulness of our model using nine in-house designs. Information on these designs as well as model's accuracy is presented below:

Design	Cell count	Area	Approximate Typical Flow-Time: From place to route with clock	Model Accuracy (DNN)	Model Accuracy (Decision Tree)
Design-1	780,000	205,000	110 Hours	94.20%	89.01%
Design-2	675,000	115,000	80 Hours	91.72%	89.22%
Design-3	310,000	64,000	40 Hours	92.96%	90.94%
Design-4	343,000	75,000	50 Hours	92.86%	88.84%
Design-5	454,000	108,000	100 Hours	93.49%	90.42%
Design-6	197,000	30,000	30 Hours	93.68%	90.50%
Design-7	255,000	77,000	35 Hours	94.57%	86.98%
Design-8	380,000	78,000	50 Hours	92.33%	90.05%
Design-9	690,000	362,000	65 Hours	92.03%	87.37%
Average				93.09%	89.26%

- As evident, Deep Neural Network (DNN) gives us the best set of accuracy. For the DNN, we use three hidden layers with respectively 16, 20 and 16 neurons.

- We also handpicked corner cases, for which routed comparison disagreed with the placed comparison. Our CompareApp correctly predicted 23 of 25 such cases.

Conclusion / Future Work

- We propose an ML-based technique, CompareApp, which can use placed information to predict a better run out of a set of runs
- We got 92%-95% accuracy across the nine designs that we investigated. Deep Neural Network (DNN) based technique gave the best accuracy
- Our model works fine on the corner cases as well
- **Future Work:**
  - Extension of the model to compare more than two runs
  - Extension of the model to make comparison in regards to other metric, such as power, area, WNS
  - Extension of the model to predict better routed design immediately after the synthesis step